ECE 443

Shift Register Project #1

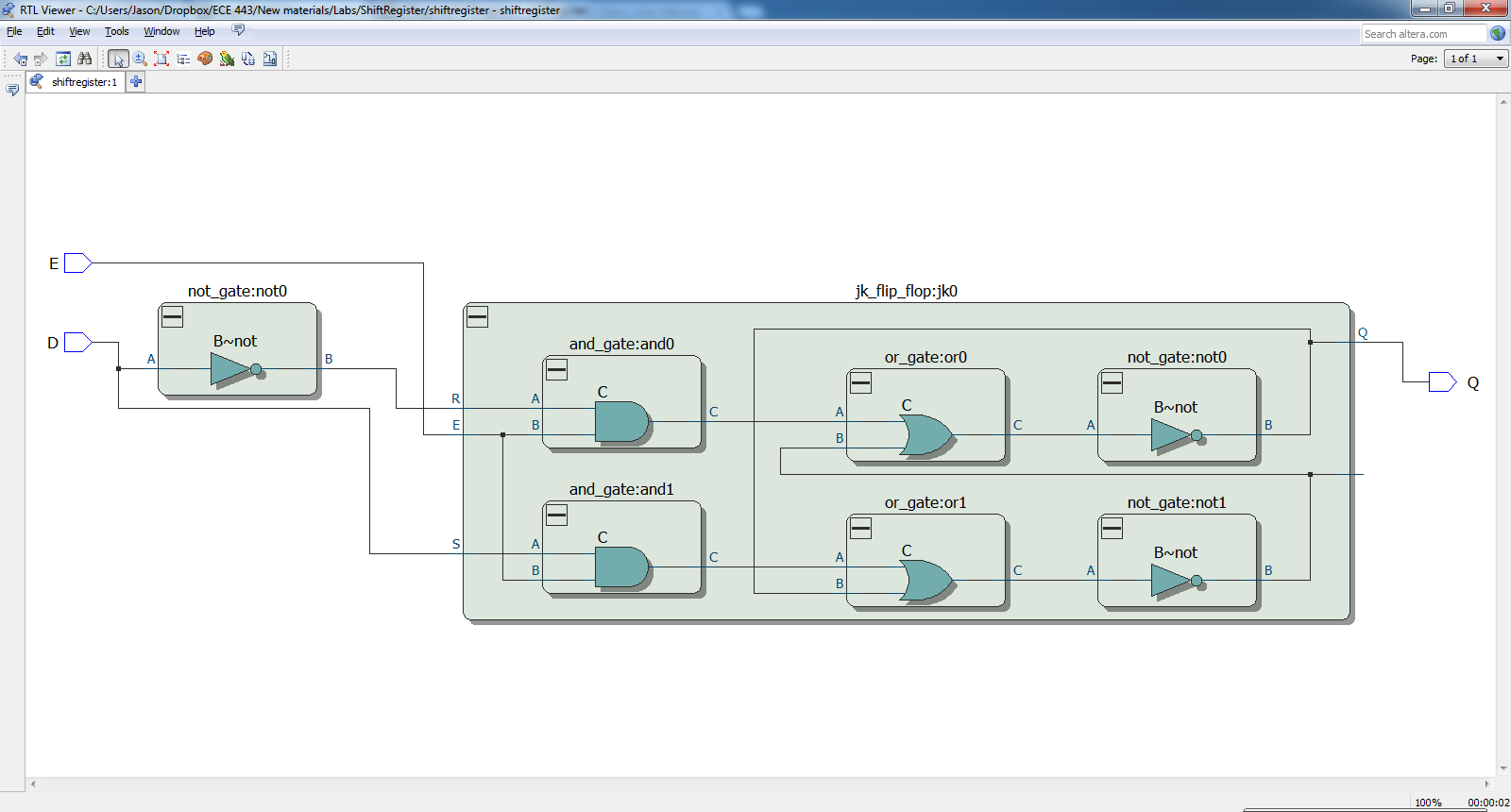
**General Guideline**

1. **Due on October 8, 11:59PM**
2. **You will receive 20 points deduction for every 12 hours late submission**
3. **You need to put the hard copy of your write-up report in my mail box (see the Section of Deliverable for details)**
4. **You need to submit your 1 VHDL Workspaces and report via Blackboard (see the Section of Deliverable for details). You have to zip them into one file and clearly name and organize them**
5. **You need to put the comments to your code**
6. **This is an individual lab assignment**

**ALDEC will be used, not Quartus.**

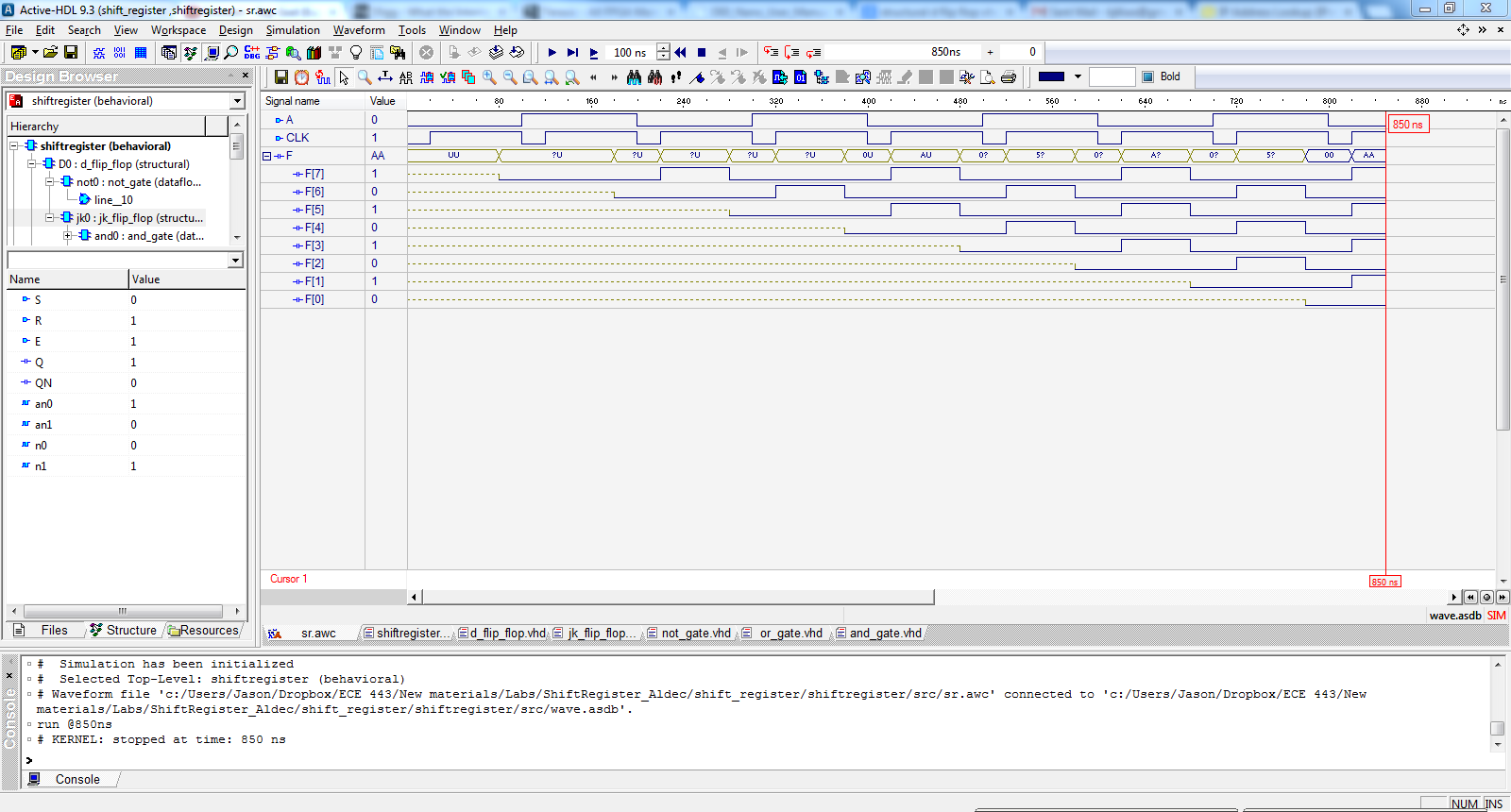
**Objective**

For this lab, you will be implementing an 8 bit shift register structurally. The easiest way to implement an 8 bit shift register, is to use 8 D flip flops. A D flip flop can be constructed using a JK flip flop and a not gate. A diagram showing the structure of a D flip flop is shown below.



When E (which stands for enable) is high, the logic value at D is stored in the flip flop and output at Q. When E is set to a logic low, the value that D was when E was high will still be output at Q. It is important to note that while if E is held high and D changes its state, Q will also do the same.

It is important to note that in order to get the shift register to work correctly you need to use a rising edge detector. Instead of implementing one, we will have to use a clock with a particular duty cycle. In this case, the clock period is 100 ns with an 80% duty cycle. Due to the timing requirements, **YOU WILL NOT BE ABLE TO USE QUARTUS. YOU MUST USE ALDEC**. The simulation should be run for 850 ns. If it works correctly, the output should resemble the image below (the value of F at 850 ns should be **AA**).



You need to implement structural VHDL code for the and gate, or gate, not gate, JK flip flop and D flip flop. Additionally, you have to create an eight bit shift register structurally using VHDL.

**You also need to implement an output called DONE that goes high after 8 clock cycles. Only this part does not need to be done structurally.**

**Deliverable/Grading:**

1. VHDL Workspace: Implementation of an 8 bit shift register and output that goes high after 8 clock cycles(50 points)
2. Reports: Write up a report including a screen shot of simulation that can validate your answer and explain how the simulation of the shift register is correct in your code works (50 points)
   1. Need to detail how you implement your project. For example: what you entry point are, what those functions mean, how you relate those codes to the circuit, what those parameters mean, how you generate the result.